Exhibit 31

1	UNITED STATES PATENT AND TRADEMARK OFFICE		
2	BEFORE THE PATENT TRIAL AND APPEAL BOARD		
3			
4			
5	Samsung Electronics Co. Ltd. Case No. IPR2022-01427		
6	Petitioner, Patent No. 9,318,160		
7	vs.		
8	Netlist, Inc., Case No. IPR2022-01428		
9	Patent Owner. Patent No. 8,787,060		
10	/		
11			
12			
13	VIDEOCONFERENCE DEPOSITION OF ANDREW WOLFE, Ph.D.		
14	Tuesday, June 27, 2023		
15	Volume I (Pages 1 - 191)		
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23	Reported Remotely and Stenographically by:		
24	JANIS JENNINGS, CSR No. 3942, CLR, CCRR		
25	Job No. 5965315		
	Page 1		

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1		1	INDEX	
2		2	11,221	
3		3	WITNESS PAGE	
4		4	ANDREW WOLFE, Ph.D.	
5		5	VOLUME I (Pages 1 - 191)	
6		6	VOLUME I (Lages 1 - 171)	
7	DEPOSITION OF ANDREW WOLFE, Ph.D.,	7	EXAMINATION BY MS. ZHONG	6
8	appearing remotely, located in Santa Clara,	8	LAAMINATION DT MS. ZHONG	U
9	California, taken on behalf of the Petitioner,	9		
10		10		
	beginning at 8:58 a.m., on Tuesday, June 27,			
11	2023, sworn remotely by Janis Jennings, Certified	11		
12	Shorthand Reporter No. 3942, CCRR, located in the	12		
13	City of Walnut Creek, County of Contra Costa,	13		
14	State of California.	14		
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21		21		
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23		23		
24		24		
25		25		
	Page 2			Page 4
1 2	REMOTE APPEARANCES:	1 2	EXHIBITS	
3	For the Patent Owner Netlist, Inc.:	3	EXHIBIT PAGE	
4	IRELL & MANELLA LLP	4	Exhibit 1014 Patent Application 2011/0103156	44
5	BY: H. ANNITA ZHONG, ESQ.	5	Kim et al.	44
6	1800 Avenue of the Stars	6	Exhibit 1015 United States Patent 8,041,881	98
7	Suite 900			90
		7	Ranjan et al.	_
8 9	Los Angeles, California 90067 310.277.1010	8 9	Exhibit 1016 Patent Application 2011/0026293 Riho	6
10	hzhong@irell.com	10	Exhibit 1017 United States Patent 7,969,192	125
11		11	Wyman et al.	
12	For the Petitioner Samsung Electronics Co., Ltd.:	12	Exhibit 1024 United States Patent 7,796,446	100
13	BAKER BOTTS LLP	13	Ruckerbauer et al.	
14				
	BY: THEODORE W. CHANDLER, ESQ.	14	Exhibit 1026 Patent Application 2006/0277355	18
15		14 15	Exhibit 1026 Patent Application 2006/0277355 Ellsberry et al.	18
15	FERENC PAZMANDI, Patent Agent	15	Ellsberry et al.	18 55
			Ellsberry et al. Exhibit 2100 Modified Kim Figure 3	
15 16 17	FERENC PAZMANDI, Patent Agent 101 California Street Suite 3200	15 16	Ellsberry et al. Exhibit 2100 Modified Kim Figure 3 Exhibit 2101 Paper titled " A 1.2V 54Gb/x	55
15 16 17 18	FERENC PAZMANDI, Patent Agent 101 California Street Suite 3200 San Francisco, California 94111	15 16 17 18	Ellsberry et al. Exhibit 2100 Modified Kim Figure 3 Exhibit 2101 Paper titled " A 1.2V 54Gb/x HBM2 Stacked DRAM with Spiral	55
15 16 17 18 19	FERENC PAZMANDI, Patent Agent 101 California Street Suite 3200 San Francisco, California 94111 415.291.6200	15 16 17 18 19	Ellsberry et al. Exhibit 2100 Modified Kim Figure 3 Exhibit 2101 Paper titled " A 1.2V 54Gb/x HBM2 Stacked DRAM with Spiral Point-to-Point TSV Structure and	55
15 16 17 18 19 20	FERENC PAZMANDI, Patent Agent 101 California Street Suite 3200 San Francisco, California 94111	15 16 17 18 19 20	Ellsberry et al. Exhibit 2100 Modified Kim Figure 3 Exhibit 2101 Paper titled " A 1.2V 54Gb/x HBM2 Stacked DRAM with Spiral	55
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15 16 17 18 19 20 21 22	FERENC PAZMANDI, Patent Agent 101 California Street Suite 3200 San Francisco, California 94111 415.291.6200	15 16 17 18 19 20 21 22	Ellsberry et al. Exhibit 2100 Modified Kim Figure 3 Exhibit 2101 Paper titled " A 1.2V 54Gb/x HBM2 Stacked DRAM with Spiral Point-to-Point TSV Structure and	55
15 16 17 18 19 20 21 22 23	FERENC PAZMANDI, Patent Agent 101 California Street Suite 3200 San Francisco, California 94111 415.291.6200	15 16 17 18 19 20 21 22 23	Ellsberry et al. Exhibit 2100 Modified Kim Figure 3 Exhibit 2101 Paper titled " A 1.2V 54Gb/x HBM2 Stacked DRAM with Spiral Point-to-Point TSV Structure and	55
15 16 17 18 19 20 21 22 23 24	FERENC PAZMANDI, Patent Agent 101 California Street Suite 3200 San Francisco, California 94111 415.291.6200	15 16 17 18 19 20 21 22 23 24	Ellsberry et al. Exhibit 2100 Modified Kim Figure 3 Exhibit 2101 Paper titled " A 1.2V 54Gb/x HBM2 Stacked DRAM with Spiral Point-to-Point TSV Structure and	55
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1 different bit values? 09:45	1 same logic rank? Can you do that? 09:48
2 MR. CHANDLER: Objection. Form. 09:45	2 MR. CHANDLER: Objection. Form. 09:48
3 BY MS. ZHONG: 09:45	3 THE WITNESS: I don't know. That's not 09:48
4 Q. For example, one is outputting 1, the other 09:45	4 BY MS. ZHONG:
5 is outputting 0, then the signal can't be 09:45	5 Q. Not really okay. Not can you do that, 09:48
6 transmitted correctly, there is going to be 09:45	6 but would a POSITA do that? 09:48
7 collision? 09:45	7 MR. CHANDLER: Objection. Form. 09:48
8 MR. CHANDLER: Objection. Form. 09:45	8 DEPOSITION REPORTER: Can you repeat your 09:48
9 THE WITNESS: Again, that is not the actual 09:45	9 question, please. 09:48
10 configuration of Riho, but that would be one of the 09:45	10 BY MS. ZHONG: 09:48
11 possible problems that could occur if you were to 09:45	11 Q. What if D14 and D15 belonged to two 09:48
12 try to connect D15 and D14 both to the same TSV and 09:45	12 different ranks so they don't operate 09:48
13 allow them to output at the same time. But again 09:45	13 simultaneously, would a POSITA make such a 09:48
14 BY MS. ZHONG: 09:46	14 configuration? 09:48
15 Q. What other problems okay. 09:46	15 A. I don't think they would start with Riho to 09:48
What other problems would there be if you 09:46	16 do that. Again, there are lots of different kinds 09:49
17 connected D15 and D14 to the same TSV and allow them 09:46	17 of memory configurations that a POSITA knows how to 09:49
18 to output data simultaneously? 09:46	18 do and can make work properly. 09:49
19 MR. CHANDLER: Objection. I don't think he 09:46	19 I would have to look at a complete design to 09:49
20 finished his previous answer. 09:46	20 understand what the impact would be of making that 09:49
21 THE WITNESS: I did. 09:46	21 kind of a change, but you wouldn't make that change 09:49
But one of the problems, there could be 09:46	22 without making other changes as well. 09:49
23 speed-related problems. There could be 09:46	23 Q. What other change would you make? 09:49
24 current-related problems. There could be damage to 09:46	24 MR. CHANDLER: Objection. Form. 09:49
25 circuits. Again, that's not the way Riho is 09:46	25 Incomplete. 09:49
Page 30	Page 32
1 designed. So 09:46	1 THE WITNESS: I don't know. I would have to 09:49
2 BY MS. ZHONG:	2 think it through. 09:49
3 Q. I understand. 09:46	3 Again, I'm not going to try to design a 09:49
When you say there could be "speed-related 09:46	4 complete working memory system based on a 09:49
5 problems," what problems are you referring to in 09:46	5 hypothetical sitting here today. But you would make 09:49
6 specific? 09:46	6 sure you had the appropriate control signals and the 09:49
7 A. Again, that's not the way Riho was designed 09:46	7 appropriate bus switching and you would analyze the 09:49
8 and it's not a design that makes any sense. So if 09:46	8 timing and the electrical operation and you would 09:49
9 one were to do it in practice, one would make other 09:46	9 make it work. 09:49
10 changes as well to make it work. 09:47	10 BY MS. ZHONG: 09:49
But Riho treats D14 and D15 as two parts of 09:47	11 Q. Would that involve substantial redesign or 09:49
12 the same data work. Each one supplies 32 bits. 09:47	12 just a little bit of work? 09:49
13 They are operated at the same time and each of one 09:47	13 MR. CHANDLER: Objection. Form. 09:50
14 requires 32 wires to communicate those 32 bits. 09:47	14 THE WITNESS: I don't know until I try it. 09:50
15 That's its mode of operation. 09:47	15 Again, I wouldn't start from Riho and make that 09:50
16 If you were to redesign it, you would have 09:47	16 particular change because it really doesn't seem to 09:50
17 to make some substantial changes to to change the 09:47	17 be something that Riho was contemplating. There are 09:50
18 way that it operates to make sure that it operates 09:47	18 lots of other modifications one can make to Riho, 09:50
19 correctly and effectively. You couldn't just only 09:47	19 but making D14 and D15 not operate simultaneously 09:50
20 connect D14 and D15 to the same set of vias without 09:47	
21 any other changes and expect it to operate 09:47	21 point for. 09:50
22 correctly. 09:47	22 BY MS. ZHONG: 09:50
23 Q. What if D14 and D15 belonged to two 09:47	23 Q. And you said you would not start with Riho. 09:50
24 different ranks, so they don't operate 09:48	24 Is it because in Riho, D15, D14, et cetera, belong 09:50
25 simultaneously but belong, say, for example, to the 09:48 Page 31	25 to the same rank and they are intended to operate 09:51 Page 33
1 age 31	1 age 33

1 simultaneously? 09:51	1 BY MS. ZHONG: 09:54
2 MR. CHANDLER: Objection. Form. 09:51	2 Q. Okay. I thought a rank is a collection of 09:54
3 THE WITNESS: In Riho's preferred 09:51	3 DRAMs that respond to a common memory command 09:54
4 embodiment, D0 through D7 are part of the same rank 09:51	4 simultaneously. That's not your understanding of 09:54
5 and D8 through D15 are part of a second rank, and 09:51	5 what rank is? 09:54
6 that's the way his preferred embodiment works. 09:51	6 MR. CHANDLER: Objection. Form. 09:54
7 BY MS. ZHONG: 09:51	7 THE WITNESS: That is my understanding. 09:54
8 Q. Okay. What's the significance of belonging 09:51	8 But I think in common usage, one would still call 09:54
9 to the same rank? 09:51	9 something a rank if it had that capability but also 09:54
10 A. I'm not sure I understand the question. 09:51	10 had the capability to do a partial read. 09:54
11 Q. You said in Riho's preferred embodiment, 09:51	11 BY MS. ZHONG: 09:54
12 D0 through D7 are part of the same rank, and D8 09:51	12 Q. Where does that definition come from? 09:54
13 through D15 are part of the second rank, and that's 09:51	13 MR. CHANDLER: Objection. Form as to the 09:54
14 the way his preferred embodiment works. 09:51	14 question there. 09:55
15 So my question to you is: What is 09:52	15 THE WITNESS: I just think that's common 09:55
16 significant that D8 for example, D8 through D15 09:52	16 usage, right? If a if a rank can provide data 09:55
17 are part of one rank and D0 through D7 belongs to 09:52	17 simultaneously from each DRAM chip, I don't think it 09:55
18 another rank? 09:52	18 has to in every instance for a person of ordinary 09:55
19 A. Again, I don't understand the question. I 09:52	19 skill to refer to it as a rank. 09:55
20 was answering your previous question about how the 09:52	20 BY MS. ZHONG: 09:55
21 ranks were organized. 09:52	21 Q. So you think "rank" can refer to a set of 09:55
22 Q. Okay. So if the dies belong to the same 09:52	22 family devices that read or write less than a full 09:56
23 rank, what would happen if a read command is sent to 09:52	23 bit width of the memory module in response to 09:56
24 the stack array? Does that mean all eight of the 09:52	24 command signals? 09:56
25 dies in the same rank is going to output data 09:52	25 MR. CHANDLER: Objection. Form. 09:56
Page 34	Page 36
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1 simultaneously? 09:52	1 THE WITNESS: I don't think that's quite 09:56
1 simultaneously? 09:52 2 MR. CHANDLER: Objection. Form. 09:52	
1 simultaneously? 09:52 2 MR. CHANDLER: Objection. Form. 09:52 3 THE WITNESS: In the Figure 5 embodiment of 09:52	1 THE WITNESS: I don't think that's quite 09:56 2 what I said. 09:56 3 BY MS. ZHONG: 09:56
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1 simultaneously? 09:52 2 MR. CHANDLER: Objection. Form. 09:52 3 THE WITNESS: In the Figure 5 embodiment of 09:52 4 Riho, if you issue a read operation, all of the DRAM 09:52 5 die in a single rank will send data to the logic LSI 09:53	1 THE WITNESS: I don't think that's quite 09:56 2 what I said. 09:56 3 BY MS. ZHONG: 09:56 4 Q. Okay. Then can you further explain what you 09:56
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1 simultaneously? 09:52 2 MR. CHANDLER: Objection. Form. 09:52 3 THE WITNESS: In the Figure 5 embodiment of 09:52 4 Riho, if you issue a read operation, all of the DRAM 09:52 5 die in a single rank will send data to the logic LSI 09:53 6 chip simultaneously. 09:53 7 BY MS. ZHONG: 09:53	1 THE WITNESS: I don't think that's quite 09:56 2 what I said. 09:56 3 BY MS. ZHONG: 09:56 4 Q. Okay. Then can you further explain what you 09:56 5 meant? 09:57 6 A. I think I gave a pretty clear explanation, 09:57 7 but I will try one more time. 09:57
1 simultaneously? 09:52 2 MR. CHANDLER: Objection. Form. 09:52 3 THE WITNESS: In the Figure 5 embodiment of 09:52 4 Riho, if you issue a read operation, all of the DRAM 09:52 5 die in a single rank will send data to the logic LSI 09:53 6 chip simultaneously. 09:53	1 THE WITNESS: I don't think that's quite 09:56 2 what I said. 09:56 3 BY MS. ZHONG: 09:56 4 Q. Okay. Then can you further explain what you 09:56 5 meant? 09:57 6 A. I think I gave a pretty clear explanation, 09:57 7 but I will try one more time. 09:57
1 simultaneously? 09:52 2 MR. CHANDLER: Objection. Form. 09:52 3 THE WITNESS: In the Figure 5 embodiment of 09:52 4 Riho, if you issue a read operation, all of the DRAM 09:52 5 die in a single rank will send data to the logic LSI 09:53 6 chip simultaneously. 09:53 7 BY MS. ZHONG: 09:53 8 Q. Is that how DRAMs are supposed to operate, 09:53	1 THE WITNESS: I don't think that's quite 09:56 2 what I said. 09:56 3 BY MS. ZHONG: 09:56 4 Q. Okay. Then can you further explain what you 09:56 5 meant? 09:57 6 A. I think I gave a pretty clear explanation, 09:57 7 but I will try one more time. 09:57 8 A rank of memory in the way that we 09:57 9 ordinarily use that term is capable of providing an 09:57
1 simultaneously? 09:52 2 MR. CHANDLER: Objection. Form. 09:52 3 THE WITNESS: In the Figure 5 embodiment of 09:52 4 Riho, if you issue a read operation, all of the DRAM 09:52 5 die in a single rank will send data to the logic LSI 09:53 6 chip simultaneously. 09:53 7 BY MS. ZHONG: 09:53 8 Q. Is that how DRAMs are supposed to operate, 09:53 9 all the dies in the rank is supposed to respond to a 09:53 10 read signal and operate output data simultaneously? 09:53	1 THE WITNESS: I don't think that's quite 09:56 2 what I said. 09:56 3 BY MS. ZHONG: 09:56 4 Q. Okay. Then can you further explain what you 09:56 5 meant? 09:57 6 A. I think I gave a pretty clear explanation, 09:57 7 but I will try one more time. 09:57 8 A rank of memory in the way that we 09:57 9 ordinarily use that term is capable of providing an 09:57 10 output on a read from every memory die or every 09:57
1 simultaneously? 09:52 2 MR. CHANDLER: Objection. Form. 09:52 3 THE WITNESS: In the Figure 5 embodiment of 09:52 4 Riho, if you issue a read operation, all of the DRAM 09:52 5 die in a single rank will send data to the logic LSI 09:53 6 chip simultaneously. 09:53 7 BY MS. ZHONG: 09:53 8 Q. Is that how DRAMs are supposed to operate, 09:53 9 all the dies in the rank is supposed to respond to a 09:53 10 read signal and operate output data simultaneously? 09:53	1 THE WITNESS: I don't think that's quite 09:56 2 what I said. 09:56 3 BY MS. ZHONG: 09:56 4 Q. Okay. Then can you further explain what you 09:56 5 meant? 09:57 6 A. I think I gave a pretty clear explanation, 09:57 7 but I will try one more time. 09:57 8 A rank of memory in the way that we 09:57 9 ordinarily use that term is capable of providing an 09:57 10 output on a read from every memory die or every 09:57
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1 simultaneously? 09:52 2 MR. CHANDLER: Objection. Form. 09:52 3 THE WITNESS: In the Figure 5 embodiment of 09:52 4 Riho, if you issue a read operation, all of the DRAM 09:52 5 die in a single rank will send data to the logic LSI 09:53 6 chip simultaneously. 09:53 7 BY MS. ZHONG: 09:53 8 Q. Is that how DRAMs are supposed to operate, 09:53 9 all the dies in the rank is supposed to respond to a 09:53 10 read signal and operate output data simultaneously? 09:53 11 MR. CHANDLER: Objection. Form. 09:53 12 THE WITNESS: It depends on the particular 09:53	1 THE WITNESS: I don't think that's quite 09:56 2 what I said. 09:56 3 BY MS. ZHONG: 09:56 4 Q. Okay. Then can you further explain what you 09:56 5 meant? 09:57 6 A. I think I gave a pretty clear explanation, 09:57 7 but I will try one more time. 09:57 8 A rank of memory in the way that we 09:57 9 ordinarily use that term is capable of providing an 09:57 10 output on a read from every memory die or every 09:57 11 memory element in the rank simultaneously, but we 09:57 12 would still in normal usage still call it a rank if 09:57
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1 simultaneously? 09:52 2 MR. CHANDLER: Objection. Form. 09:52 3 THE WITNESS: In the Figure 5 embodiment of 09:52 4 Riho, if you issue a read operation, all of the DRAM 09:52 5 die in a single rank will send data to the logic LSI 09:53 6 chip simultaneously. 09:53 7 BY MS. ZHONG: 09:53 8 Q. Is that how DRAMs are supposed to operate, 09:53 9 all the dies in the rank is supposed to respond to a 09:53 10 read signal and operate output data simultaneously? 09:53 11 MR. CHANDLER: Objection. Form. 09:53 12 THE WITNESS: It depends on the particular 09:53 13 design. 09:53 14 BY MS. ZHONG: 09:53	1 THE WITNESS: I don't think that's quite 09:56 2 what I said. 09:56 3 BY MS. ZHONG: 09:56 4 Q. Okay. Then can you further explain what you 09:56 5 meant? 09:57 6 A. I think I gave a pretty clear explanation, 09:57 7 but I will try one more time. 09:57 8 A rank of memory in the way that we 09:57 9 ordinarily use that term is capable of providing an 09:57 10 output on a read from every memory die or every 09:57 11 memory element in the rank simultaneously, but we 09:57 12 would still in normal usage still call it a rank if 09:57 13 it also had the capability of only providing a 09:57 14 portion of the memory word. 09:57
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1 A. Tel have to look at the specifies. I think 10:02 2 A. No. I didn't – there are no memory modules 09:59 3 really that I can recall in this IPR at all. But 09:59 4 even in that case, that was not what my testimony 09:59 5 was. 09:59 6 Q. Okay. So let's say 8 dies are outputting 09:59 8 one of the operation, only 8 bits are outputting 09:59 8 one of the operation, only 8 bits are output. How 09:59 9 many – how many dies are there in the rank? Still 09:59 10 8 or only 1? 09:59 11 A. S. If the 8 dies normally objective the same of the operation of the same objection. Form. 10:00 13 additional operation in which only one operates does 10:00 14 not make the 8 stop being a rank. 10:00 15 Q. You said in normally outputs 64 bits, but 10:00 16 what if there are no what you call the normal – 10:00 17 each operation is of variable length – 10:00 18 MR. CHANDLER: Objection. 10:00 19 BY MS. ZHONG: 10:00 22 MR. CHANDLER: Objection of 10:00 23 stop of the same objection of 10:00 24 such a situation, so I don't know what a person of 10:00 25 ordinary skill would call it. I would have to look of sometimes it's 16 bits, sometimes it's 12 bits, 10:00 28 yes have the output das situations. You 10:01 29 BY MS. ZHONG: 10:00 20 MR. CHANDLER: Objection of 10:00 3 Q. So lef's say in the read operation, 10:00 4 sometimes it's 16 bits, sometimes it's 32 bits, 10:00 5 yes max configured. 10:01 10 yes max configured. 10:01 11 yes max configured. 10:01 12 Be tordinarily we would refer to the 10:01 13 Q. So if two dies hedong to the same physical rank of the die is by 8? 10:00 10 yes max configured. 10:01 10 yes max configured. 10:01 10 yes max configured. 10:01 11 yes max configured. 10:01 12 Be tordinarily we would refer to the 10:01 13 Q. So if two dies hedong to the same physical rank and logical rank. 10:04 10 yes max configured. 10:01 10 ye		
3 even in that case, that was not what my testimony 09:59	1 single die constitutes the rank; is that right? 09:59	1 A. I'd have to look at the specifics. I think 10:02
3 even in that case, that was not what my testimony 09:59	2 A. No. I didn't there are no memory modules 09:59	2 it would generally be difficult to have two die both 10:02
4 even in that case, that was not what my testimony 09:59 5 was. 09:59 5 was. 09:59 6 explained 09:59 6 explained 09:59 7 explained 09:59 6 explained 09:59 7 explained 09:59 7 explained 09:59 7 explained 09:59 8 explained 09:59 9 many - how many dies are there in the rank? Still 09:59 9 many - how many dies are there in the rank? Still 09:59 10 & or only 1? 10 & or on	-	
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6 Q. Okay. So let's say 8 dies are outputting		
7 64 bits from the memory system. Okay? And if for 09-59 8 one of the operation, only 8 bits are output. How 09-59 9 onary – how many these are there in the rank? Still 09-59 10 8 or only 1? 10 8 or only 1? 11 A. 8. If the 8 dies normally operate together 09-59 12 and output 64 bits, the fact that there is an 10-00 13 additional operation in which only one operates does 10-00 14 and output 64 bits, the fact that there is an 10-00 15 Q. You said it normally outputs 64 bits, but 10-00 16 what if there are no what you call the normal — 10-00 16 what if there are no what you call the normal — 10-00 18 MR. CHANDLER: Objection.		
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